REMARKS

In response to the Office Action mailed July 8, 2003, Applicant respectfully requests reconsideration. To further the prosecution of the application, amendments have been made in the claims, the written description, and the drawings. The application as presented is believed to be in allowable condition.

IN THE DRAWINGS

In response to ¶ 3 of the Office Action, Applicant has modified Figure 3 to address the Draftsperson's objection that the lines, numbers and letters were not uniformly thick nor well defined. The line quality of Figure 3 has been improved to overcome the Draftsperson's rejection. No new matter has been added by this change. Applicant encloses a "Request for Corrections, Approval and Entry of Drawings" letter requesting the replacement of Figure 3 with the drawing in the Appendix of this response.

IN THE WRITTEN DESCRIPTION OF THE SPECIFICATION

In ¶ 4-1, the Office Action objects to the description at lines 7-9 of page 8. The specification has been amended at lines 7-9 of page 8 to remove the reference to a "second system" and to clarify that the sentence refers to a relationship between a reverse system and a real system. No new matter has been added by this amendment because the specification on page 7, lines 8-9 discloses that the pre-image of the reverse system will be the post-image of the original system and it is clear from Figure 3 that the original system refers to the real machine (i.e., the real system).

In ¶ 5, the Office Action objects to the incorporation by reference of Applicant's British application on page 5, stating that such incorporation is improper because it incorporates essential material. Applicant respectfully disagrees that any of the incorporated material is "essential," as none is necessary to describe or enable the claimed invention, nor to describe the best mode. MPEP § 608.01(p)(I)(A). Thus, Applicant's published British Application (No 9624935.4) is nonessential material and appropriate for incorporation by reference pursuant to MPEP § 608.01(p)(I)(A).

IN THE CLAIMS

Claim Objections

Applicant notes the objection in ¶ 6 of the Office Action to the claim order, but because prosecution of the application is ongoing, Applicant believes that no amendment regarding claim sequence is appropriate until allowance. MPEP 608.01(n)IV.

1. Claims 1-21 Satisfy Requirements of 35 U.S.C. § 112, First Paragraph

Claims 1-21 stand rejected under 35 U.S.C. § 112, first paragraph. Applicant respectfully traverses this rejection.

A. Any Errors In The Equations Are Not Fatal Under §112, ¶1

In ¶ 8-1, the Office Action asserts that the equations on pages 5 and 6 are "obviously incorrect" so that one skilled in the art could not make or use the invention without undue experiment. Applicant respectfully disagrees.

Initially, the equations are merely examples of functions that could be used (page 4, lines 3-16, page 6, line 23-page 7, line 19, and page 9, lines 1-3). Thus, it is respectfully asserted that the specification enables the invention even without any equations. In addition, Applicant respectfully asserts that one of skill in the art could still practice the disclosed embodiments of the invention despite the "obvious errors" in the equations of the disclosed embodiment. As the Office Action pointed out, the errors are "obvious," as the equations clearly are missing unpaired parentheses or equal signs. One of skill in the art would not only recognize that these errors are present (just as the Examiner did), but would recognize what the errors were and what equations were intended, as the errors are clearly typos that one skilled in the art would recognize.

Specifically, the last line of page 5 is written as follows:

b0' = (NOT b0'' AND NOT [b0=1]) OR b0'' AND [b0=0])

It is clear that the equation above is missing a parenthesis, and it is clear that the parenthesis must be immediately after the OR, as no other location would make sense. Thus, one skilled in the art would understand that the proper equation is:

b0' = (NOT b0'' AND NOT [b0=1]) OR (b0'' AND [b0=0])

The Office Action also recognized that some of the errors in the equations were due to missing equal signs. Specifically, the equation at line 3 on page 6 is as follows:

b1 (b0 AND b1') OR (NOT b0 AND NOT b1')

It is clear that the equation above is missing an equal sign and one skilled in the art would have recognized that the equal sign belongs immediately after b1, and would read the equation as:

b1 = (b0 AND b1') OR (NOT b0 AND NOT b1')

The equation on line 4 of page 6 reads as follows:

(b1') AND [b0=b1]) OR (NOT b1' AND NOT [b0=b1])

One skilled in the art would have immediately recognized that there is one too many close parentheses ")," and that the parenthesis after the first occurrence of b1' should not be there because there is no need for parentheses around solely a single element grouped by itself. As such, one skilled in the art would read the equation as:

(b1' AND [b0=b1]) OR (NOT b1' AND NOT [b0=b1])

The equation on line 7 of page 6 reads as follows:

b1' = (NOT bill AND [b0=b1]) OR (b1'' AND [b0=b1]) thus bl' = [b0=b1]

One skilled in the art would have recognized that the word bill was a typo, and also would have realized that bill should read as b1'' because b1'' is absent from the left side of the OR, such that the equation does not follow the format of the other equations. Specifically, all of the previous equations in the application follow a similar format, namely, the same set of variables (albeit with different negation operations) appear on both sides of the OR. As such, one skilled in the art would read the equation as:

b1' = (NOT b1'' AND [b0=b1]) OR (b1'' AND [b0=b1]) thus bl' = [b0=b1]

In view of the foregoing, Applicant submits that one of skill in the art would recognize not only that there are errors in the equations, but also what the intended equations were so that the skilled artisan can practice the disclosed embodiment without any experimentation. For this additional reason, it is requested that the rejection under §112, ¶1 be withdrawn.

B. Applying A Constraint To Transitions Of The Reverse Model Does Not Render The Disclosure Unclear

In ¶ 8-2, the Office Action asserts that the individual transitions determine the relationship between the individual states, citing the example on page 4 as representative of

showing that the transition from state S1 to state S2 is T12. The Office Action states that "all transitions of the reverse model have already characterized the reverse model completely" so that any modification of any transition would result in a different reverse model. In view of that, the Office Action concludes that it is unclear how to apply a parameterization of the constraint to all transitions of the reverse model without eventually altering the reverse model. Applicant respectfully disagrees.

It is important to keep in mind the difference between "transitions" and "transition functions". A few examples illustrate the difference. In the example referred to in the Office Action, transition T12 represents the transition from state S1 to state S2, while transition T21 represents the reverse transition from state S2 to state S1 (page 4, lines 17-19). The labels T12 and T21 merely represent transitions between two states, they do not describe the functional relationship between the states. It is a transition function that defines the functional relationship between two states.

In the above examples, different transition functions are determined for the original model (e.g., up counter) and the reverse model (e.g., down counter) (page 5, line 7-page 6, line 22). Specifically, for the original model in the first example (T12), if the machine is at state S1, a transition function that results in a transition from S1 to S2 is identified. The transition function defines what must be done to the bits of the state machine to achieve the transition (see e.g., page 4, line 23-page 5, line 1). For the reverse model at the same starting state, a different transition function is identified, namely one that results in the reverse model transitioning from state S1 to state S0. This transition function defines different operations on the bits of the state machine.

As should be clear from the foregoing, transitions are different from transition functions. It is transition functions, not transitions, that describe the functional relationship between the states (page 6, line 12). This difference is further emphasized in Figure 3 where "transitions" are extracted at step 1001, and "transition functions" are extracted at step 1003. Therefore, contrary to the assertions in the Office Action, all transitions of the reverse model do not completely characterize the reverse model, as the transition functions also are necessary.

The Office Action states that any modification of any transition will eventually form a different reverse model. This reflects a misunderstanding of the quoted section of the

specification, which does not describe modifications to transitions, but applying a parameterization of the constraints to transitions to arrive at the transition functions for the reverse model. According to one aspect of Applicant's invention, the present invention derives transition functions for a reverse machine (page 1, lines 25-26). The reverse transition functions generally will be different from the real state machine transition functions. Figure 3 shows that "transition functions" are transformed into constraints at step 1007 and a parameterization of the constraints is applied at stage 1008 to the reverse transitions to thereby form the model of the reverse machine at step 1010 (page 8, lines 15-22). Thus, the transition functions of the real machine are processed so as to transform the transition functions of the real machine into constraints and a parameterization of those constraints is applied to the reverse transitions to form the model of the reverse machine (page 8, lines 19-22). Hence, there is no modification of the transitions of the reverse model. Rather, the transition functions of the original system are used to constrain the transitions of the reverse system (page 7, lines 12-14). Moreover, the estimated transition function of the reverse model of the system is derived from knowledge of the next state variable of the reverse system which corresponds to the previous state variables of the original system (page 7, lines 21-24). Therefore, the formation of the reverse model may include transforming a transition function of the control system into a constraint on the reverse model, and applying a parameterization of said constraint to all transitions of the reverse model. This process does not alter the reverse model as alleged in the Office Action.

As should be clear from the foregoing, the disclosure is believed to be sufficiently clear to enable a person skilled in the art to carry out the invention.

C. The Specification Does Not Disclose Introducing Inputs Into State Variables

The written description recites that "the logical device is constructed and arranged to *substitute* the state variable of the reverse model by the transition functions of the reverse model to provide a new set of states representing the pre-image of the reverse model, and thus provide the post-image in the system." (page 3, lines 5-8) (emphasis added). The Office Action asserts that for any finite state machine, transition functions may include inputs but state variables may not. The Office Action concludes that it is unclear to one skilled in the art how to avoid introducing inputs into state variables when substituting the state variable by transition functions.

It is respectfully asserted that the Office Action misconstrues the meaning of the word "substitute" with respect to the above-quoted first paragraph on page 3. The "substitution" referred to simply means that for each constraint, the parameterization of the variables is calculated and is substituted in the transition functions and the remaining constraints (page 7, lines 15-17). This step is represented by stage 1008 in Figure 3, which shows that a parameterization of the constraints (of the transition functions) is applied to each of the state variables (reverse transitions). This step is also discussed in the 2 bit counter example of Applicant's written description, which shows that the state variables (e.g., b0 and b1) are substituted with the constraints of the transition functions (e.g., equations (1) and (2), respectively) (page 5, line 23-page 6, line 11).

For the reasons disclosed above, Applicant maintains that the disclosure raises no ambiguity for the person skilled in the art as to how to carry out the invention.

D. Claims 1 and 5-7 Have Been Amended To Recite A Reverse Model Of A "State Machine Model"

The Office Action asserts that the limitation "control system" in claims 1 and 5-7 and the limitation "electronic circuit" in claims 2-4 and 8-21 are not supported by the written description, because such description only describes a finite state machine. Claims 1 and 5-7 have been amended to recite the reverse model as being of a state machine model. Thus, it is believed that the Examiner's concern has been addressed.

2. Claims 13 and 15-19 Have Been Amended to Satisfy the Requirements of 35 U.S.C. § 112, ¶2

Claim 13 and claim 15 were rejected as lacking antecedent basis for the claim limitation "said reverse system." These claims have been amended to provide such antecedent basis so that withdrawal of the rejection of claims 13 and 15, as well as claims 16-19 that depend therefrom, under 35 U.S.C. § 112, ¶2, is respectfully requested.

Double Patenting

Claims 5-21 are rejected under the judicially-created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3 of U.S. Patent No. 6,031,983. Applicant submits herewith a terminal disclaimer with respect to U.S. Patent No. 6,031,983. Accordingly, the double patenting rejection should be withdrawn.

Claim Interpretation Issue

Claims 1 and 5-7 recite the limitation "control system," and claims 2-4 and 8-21 recite the limitation "electronic circuit." The Office Action asserts that because only a finite state machine is supported in the specification, the Examiner will interpret both "control system" and "electronic circuit" as a "finite state machine." As discussed above, the claims have been amended to refer to the reverse model as being of a state machine model of the control system or electronic circuit. Thus, it is believed that the strained interpretations suggested for the terms "control system" and "electronic circuit" are unnecessary, and Applicant respectfully requests that the Examiner acknowledge on the record that these terms will be interpreted to have their ordinary meanings, and not as reciting a finite state machine.

Rejections Under 35 U.S.C. §102

1. Claim 1

Claim 1 is rejected under 35 U.S.C. §102(b) as purportedly being anticipated by Vai et al., "Qualitatively Modeling Heterojunction Bipolar Transistors for Optimization: a Network Approach", Proceedings, IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, August 1993, pages 219-227 (herein referred to as Vai). Applicant respectfully traverses this rejection.

Applicant asserts that claim 1 as previously presented patentably distinguished over Vai. The Office Action states that Figure 4 of Vai discloses a method of synthesizing a reverse model of a control system comprising: *transforming a transition function of the control system into a constraint on the reverse model*, and applying a parameterization of said constraint to all transitions of the reverse model. Applicant respectfully disagrees.

Vai describes the development of a parallel distributed analog computing network (i.e., a neural network) for modeling the relationship between the parameters of a fabrication process

and the characteristics of a semiconductor device (specifically, a heterojunction bipolar transistor) to provide a reverse modeling process which performs device optimization (page 119, lines 17-21). Hence, Vai, unlike Applicant, is not concerned with a state machine model. Moreover, the reverse modeling process of Vai is "similar to a standard modeling procedure except that the goal . . . is to minimize the difference between the modeled and desired performance" (page 220, lines 3-5). In contrast, in the embodiment of Applicant's invention recited in claim 1, the formation of the reverse model includes transforming a transition function of a state machine of a control system into a constraint on the reverse model, and applying a parameterization of said constraint to all transitions of the reverse model (page 2, lines 8-10). This is not taught or suggested in Vai.

The Office Action places emphasis on the word "Constraints" in Figure 4. Figure 4 of Vai refers to electrical and fabrication constraints which are defined in Vai as the constraints resulting from an equivalent circuit model (e.g., KVL and KCL) and the fabrication process (e.g., doping concentration) (page 220, lines 11-13). Claim 1 specifically recites "transforming a transition function of a state machine model of the control system into a constraint on the reverse model". This is not taught or suggested by Vai.

The Office Action states that Figure 4 of Vai discloses transforming a transition function of a control system into a constraint on the reverse model, and *applying a parameterization of said constraint to all transitions of the reverse model.* Applicant respectfully disagrees.

The Office Action places emphasis on the word "Mapping Algorithm" in Figure 4. Figure 4 of Vai does not disclose a parameterization technique. Rather, it discloses a mapping algorithm directed to mapping an equivalent circuit into a corresponding neural network (Figure 4 and page 224, lines 6-7). Claim 1 recites "applying a parameterization of said constraint to all transitions of the reverse model". This is not taught or suggested in Vai.

Claim 1 has been amended to further distinguish over Vai by specifically reciting the reverse model as being a reverse model of a state machine model. Figure 4 of Vai does not recite a state machine model, but merely discloses a setup for applying the neural network model of an HBT to reverse modeling. As such, Vai does not disclose transforming a transition function of a state machine model of a control system into a constraint on the reverse model.

As should be clear from the foregoing, claim 1 is not anticipated by Vai. Accordingly, withdrawal of the rejection of claim 1 under 35 U.S.C. §102(b) is respectfully requested.

2. Claim 2

Claim 2 stands rejected under 35 U.S.C. §102(b) as being anticipated by Vai. Applicant respectfully traverses this rejection.

Claim 2 is substantially identical to claim 1, except for the recitation of the state machine model being of an electronic circuit rather than a control system. Therefore, claim 2 distinguishes over Vai for reasons similar to those discussed above in conjunction with claim 1. Thus, withdrawal of the rejection of claim 2 under 35 U.S.C. §102(b) is respectfully requested.

Claims 3-4 depend from claim 2 and are allowable for at least the same reasons. Accordingly, withdrawal of the rejection of claims 3-4 is respectfully requested.

3. Claim 5

Claims 5 stands rejected under 35 U.S.C. §102(a) as being anticipated by Wu et al., "A Massively Parallel Reverse Modeling Approach for Semiconductor Devices and Circuits", Proceedings, 1997 IEEE/Council Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, August 1997, pages 201-209. Applicant respectfully traverses this rejection.

The Office Action states that Figure 5 and page 207 of Wu disclose forming a reverse model of a control system and calculating the pre-image in the reverse model, wherein the pre-image in the reverse model is equivalent to the post-image in said control system. Applicant respectfully disagrees.

Wu is concerned with a neural network having a parallel distributed computing architecture for the design of semiconductor devices using reverse modeling techniques. Wu does not disclose a state machine model nor a device including a processing system comprising a logical device for transitioning transition functions of a state machine model into constraints on a reverse model for the state machine model. The reference to page 207 of Wu explains that the application of a neural network in reverse modeling is carried out by applying a modified backpropagation learning rule to a trained network. This passage focuses on describing the

backpropagation learning rule and does not describe forming a reverse model of a state machine model. Figure 5 of Wu shows the setup for the evaluation of the neural network reverse modeling process. Figure 5 of Wu does not show calculating the pre-image of a reverse model wherein the pre-image is equivalent to the post-image in the control system.

In view of the foregoing, claim 5 is not anticipated by Wu. Thus, claim 5 patentably distinguishes over Wu. Accordingly, withdrawal of the rejection of claim 5 under 35 U.S.C. §102(b) is respectfully requested. Claims 6-7 depend from claim 5 and are allowable for at least the same reasons. Accordingly, withdrawal of the rejection of claims 6-7 is respectfully requested.

4. Claim 8

Claims 8 stands rejected under 35 U.S.C. §102(a) as being anticipated by Wu. Applicant respectfully traverses this rejection.

Claim 8 is substantially identical to claim 5, except for the recitation of the state machine model being of an electronic circuit rather than a control system. Thus, claim 8 distinguishes over Vai for reasons similar to those discussed above in conjunction with claim 5. Therefore, withdrawal of the rejection of claim 8 under 35 U.S.C. §102(b) is respectfully requested. Claims 9-12 depend from claim 8 and are allowable for at least the same reasons. Accordingly, withdrawal of the rejection of claims 9-12 is respectfully requested.

5. Claim 13

Claim 13 stands rejected under 35 U.S.C. §102(a) as being anticipated by Wu. Applicant respectfully traverses this rejection.

Wu is concerned with a neural network having a parallel distributed computing architecture for the design of semiconductor devices using reverse modeling techniques. The "input-output" patterns, "mapping functions" and "hidden layers" disclosed on page 204 of Wu and emphasized in the Office Action are specific only to the functionality of a neural network and do not disclose a first store storing bits representative of transition functions of a state machine model of an electronic circuit; a second store storing bits representative of an estimate of transition functions of said reverse model; and a processing system comprising a

logical device for transforming said transition functions of the state machine model of the electronic circuit into constraints on said reverse model.

Thus, claim 13 patentably distinguishes over Wu. Accordingly, withdrawal of the rejection of claim 13 under 35 U.S.C. §102(b) is respectfully requested. Claims 16 and 18-19 depend from claim 13 and are allowable for at least the same reasons. Accordingly, withdrawal of the rejection of claims 16 and 18-19 is respectfully requested.

6. Claim 14

Claims 14 stands rejected under 35 U.S.C. §102(a) as being anticipated by Wu. Applicant respectfully traverses this rejection.

Wu is concerned with a neural network having a parallel distributed computing architecture for the design of semiconductor devices using reverse modeling techniques. The "input-output patterns", "neuron" and "backpropagation learning process" disclosed on pages 203 and 204 of Wu and emphasized in the Office Action are specific only to the functionality of a neural network and do not disclose, respectively, a third store storing bits representative of transition functions of a reverse model of said electronic circuit; a fourth store storing bits representative of a set of states of a state machine model of said electronic circuit; and a forming device substituting the state variables of the reverse model by the transition functions of the reverse model to provide a new set of states representing the pre-image of said reverse model, and thus provide the post-image in said electronic circuit.

Thus, claim 14 patentably distinguishes over Wu. Accordingly, withdrawal of the rejection of claim 14 under 35 U.S.C. §102(b) is respectfully requested. Claims 15, 17 and 20-21 depend from claim 14 and are allowable for at least the same reasons. Accordingly, withdrawal of the rejection of claims 15, 17 and 20-21 is respectfully requested.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below to discuss any outstanding issues relating to the allowability of the application.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
Geoff Barrett, Applicant

Richard F. Giunta, Reg. No. 36,149
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210
Telephone: (617) 720-3500

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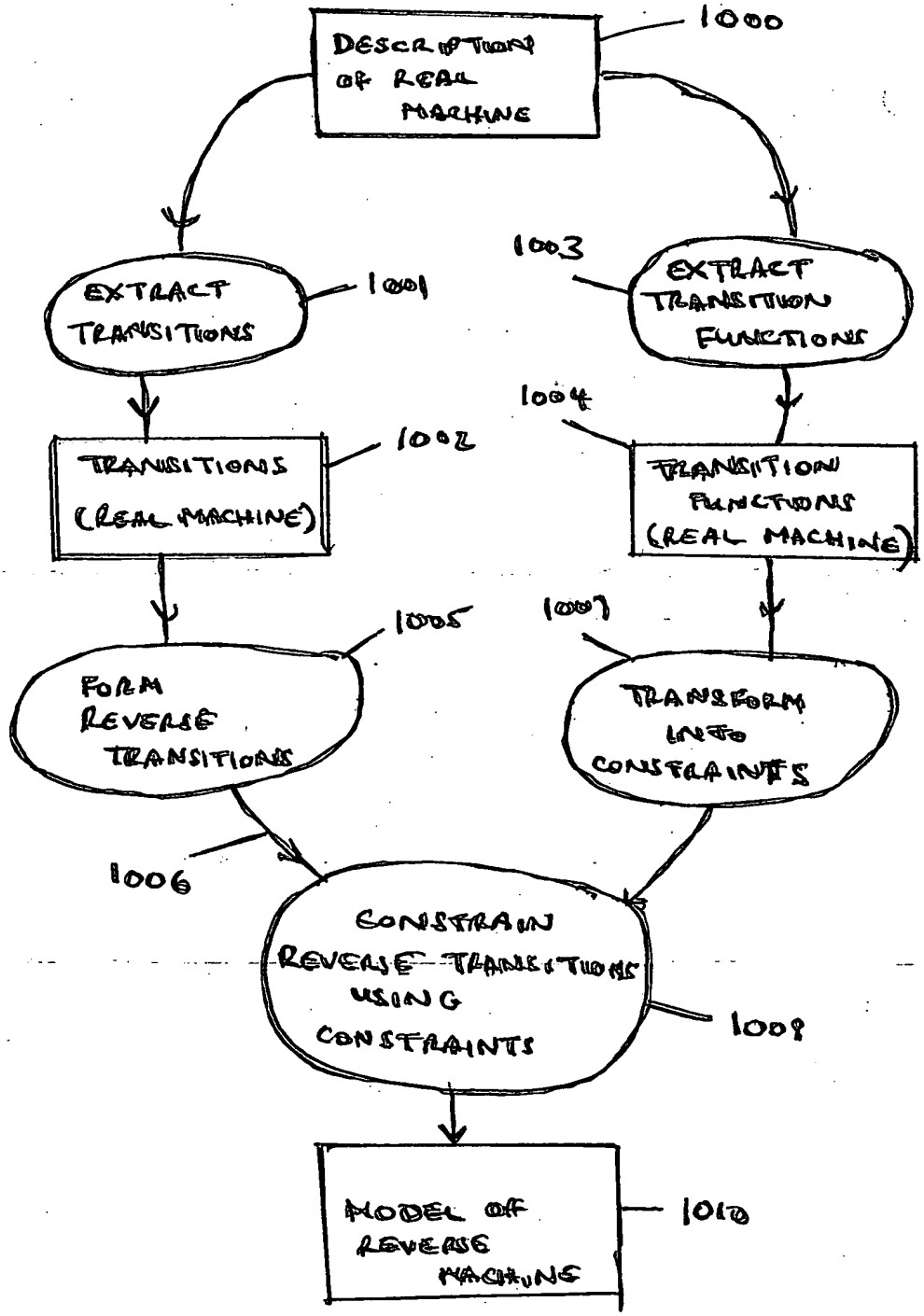

FIG 3